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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGUYEN, DUSTIN	
ART UNIT	PAPER NUMBER
2154	

DATE MAILED: 10/04/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/923,976	BRESNIKER ET AL.	
	Examiner	Art Unit	
	Dustin Nguyen	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 July 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-20 are presented for examination.

Response to Arguments

2. Applicant's arguments filed 07/03/2006 have been fully considered but they are not persuasive.

3. As per remarks, Applicants' argued that (1) Mitchell does not teach or suggest a host processor card that comprises a processor that is configured to provide a graceful shutdown signal to a graceful shutdown circuit of the host processor card, as recited in claim 1.

4. As to point (1), Mitchell discloses a host processor card configured to be fitted into a server system [i.e. a gateway card 50 in the embedded system 10] [50, Figures 2 and 3; col 4, lines 66-col 5, lines 2; and col 5, lines 19-40], a processor [i.e. the gateway card includes a debounce circuit 36] [36, Figure 3; and col 5, lines 28-30], a graceful shutdown circuit coupled to the processor and the power control line [i.e. the reset signal at 37 feeds into the shutdown and reset manager 60] [60, Figure 3; and col 5, lines 34-44], the graceful shutdown circuit configured to allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal [i.e. when the reset signal 37 is asserted, the shutdown and reset

manager 60 generates an interrupt signal on the INT input of the microprocessor 56, the shutdown of the operating system is initiated] [col 5, lines 41-55].

5. As per remarks, Applicants' argued that (2) Hamre does not teach or suggest "a switch circuit coupled to the power control line and coupled to the processor, the switch circuit configured to override a power down signal on the power control line and thereby maintain power to the host processor card if the processor has provided the graceful shutdown signal to the graceful shutdown circuit" as recited in independent claim 9.

6. As to point (2), it is rejected for similar reasons as stated in the previous Office Action. Furthermore, Hamre discloses switch S1 and the circuitry that gracefully applies power to or removes power from the circuit board power busses [Figure 7; col 7, lines 33-48; and col 8, lines 13-35].

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

8. Claims 1, 2, 6, and 8 are rejected under 35 U.S.C. 102(e) as being anticipated by Mitchell et al. [US Patent No 6,230,181].

9. As per claim 1, Mitchell discloses the invention substantially as claimed including a host processor card configured to be fitted into a server system [i.e. gateway card of plurality of cards in a communication chassis] [Figure 2; and col 3, lines 58-col 4, lines 6], the host processor card comprising:

a processor [36, Figure 3; and col 5, lines 28-30];

a memory coupled to the processor for storing an operating system [Figure 3; col 3, lines 28-34; and col 5, lines 3-18];

a power control line for controlling the power state of the host processor card [col 5, lines 34-44];

a graceful shutdown circuit coupled to the processor and the power control line [60, Figure 3; and col 6, lines 41-53], the processor configured to provide a graceful shutdown signal to the graceful shutdown circuit [i.e. the reset signal at 37 feeds into the shutdown and reset manager 60] [60, Figure 3; and col 5, lines 34-44], the graceful shutdown circuit configured to

allow a graceful shutdown of the host processor card when the power control line indicates that the host processor card is to be powered down if the processor has provided the graceful shutdown signal [i.e. when the reset signal 37 is asserted, the shutdown and reset manager 60 generates an interrupt signal on the INT input of the microprocessor 56, the shutdown of the operating system is initiated] [col 5, lines 41-55].

10. As per claim 2, Mitchell discloses wherein the graceful shutdown circuit is configured to allow an immediate shutdown of the host processor card when a received power control signal indicates that the host processor card is to be powered down if the processor has not provided the graceful shutdown signal [col 6, lines 57-65].

11. As per claim 6, Mitchell discloses wherein the processor includes a register for indicating when a graceful shutdown is to be performed, and wherein the operating system is configured to write a value to the register indicating whether a graceful shutdown is to be performed [col 1, lines 29-34].

12. As per claim 8, Mitchell discloses wherein the graceful shutdown circuit further comprises a monitor circuit coupled to the power control line and coupled to the processor, the monitor circuit configured to provide an indication of the status of the power control line to the processor [col 6, lines 22-39].

Claim Rejections - 35 USC § 103

13. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

14. Claims 3-5, 9, 11, 12, 14-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitchell et al. [US Patent No 6,230,181] in view of Hamre et al. [US Patent No 5,530,302].

15. As per claim 3, Mitchell does not specifically disclose wherein the power control line is coupled to a switch that is configured to close when the host processor card is inserted into the server system, causing the power control line to indicate that the host processor card is to be power up. Hamre discloses wherein the power control line is coupled to a switch that is configured to close when the host processor card is inserted into the server system, causing the power control line to indicate that the host processor card is to be power up [Abstract; and col 3, lines 5-19]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mitchell and Hamre because Hamre's teaching would provide hot-swapping modules for digital systems which can be inserted and removed without interrupting data bus communications [Hamre, col 2, lines 46-49].

16. As per claim 4, Hamre discloses wherein the switch is configured to open when the host processor card is being removed from the server system, causing the power control line to indicate that the host processor card is to be powered down [Abstract; col 3, lines 5-19].

17. As per claim 5, Mitchell discloses wherein the power control line is coupled to a server management card that is configured to control the power state of the host processor card via the power control line when the switch is closed [col 4, lines 7-14].

18. As per claim 9, Mitchell does not specifically disclose a switch circuit coupled to the power control line and coupled to the processor, the switch circuit configured to override a power down signal on the power control line and thereby maintain power to the host processor card if the processor has provided the graceful signal to the graceful shutdown circuit. Hamre discloses a switch circuit coupled to the power control line and coupled to the processor, the switch circuit configured to override a power down signal on the power control line and thereby maintain power to the host processor card if the processor has provided the graceful signal to the graceful shutdown circuit [i.e. gracefully or gradually removing power] [Abstract; and col 3, lines 5-19]. It would have been obvious to a person skill in the art at the time the invention was made to combine the teaching of Mitchell and Hamre because Hamre's teaching would provide a circuit board module which can be hot-swapped without creating errors on the backplane data bus [Hamre, col 2, lines 55-58].

19. As per claim 11, it is rejected for similar reasons as stated above in claims 1, 8 and 9.

20. As per claim 12, it is rejected for similar reasons as stated above in claim 2.

21. As per claim 14, it is rejected for similar reasons as stated above in claims 1, 8 and 9.

22. As per claim 15, it is rejected for similar reasons as stated above in claim 2.

23. As per claims 16-18, they are rejected for similar reasons as stated above in claims 3-5.

24. As per claim 19, it is rejected for similar reasons as stated above in claim 6.

25. Claims 7, 10, 13 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mitchell et al. [US Patent No 6,230,181] in view of Pignolet et al. [US Patent No 6,023,148].

26. As per claim 7, Mitchell does not specifically disclose wherein the operating system is configured to write a value to the register indicating that a graceful shutdown is to be performed when the operating system boots up to a point that an immediate shutdown should not be performed. Pignolet discloses wherein the operating system is configured to write a value to the register indicating that a graceful shutdown is to be performed when the operating system boots up to a point that an immediate shutdown should not be performed [i.e. boot sequence] [Figure 16; and col 18, lines 43-67]. It would have been obvious to a person skill in the art at the time

the invention was made to combine the teaching of Mitchell and Pignolet because Pignolet's teaching would allow to prevent system corruption.

27. As per claim 10, Pignolet discloses a manual emergency switch coupled to the switch circuit, the emergency switch configured to cause immediate shutdown of the host processor card [i.e. hard reset] [col 10, lines 56-61].

28. As per claim 13, it is rejected for similar reasons as stated above in claim 10.

29. As per claim 20, it is rejected for similar reasons as stated above in claim 10.

30. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dustin Nguyen whose telephone number is (571) 272-3971. The examiner can normally be reached on flex schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Follansbee John can be reached on (571) 272-3964. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Dustin Nguyen
Examiner
Art Unit 2154